Description

STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR Si:C

BACKGROUND OF INVENTION

[0001] The present invention relates generally to structures and methods of manufacturing dislocation free stressed channels in bulk silicon and SOI (silicon on insulator) MOS (metal oxide semiconductor) devices by gate stress engineering with SiGe and/or Si:C.

[0002] Dislocations are defects in crystal structures, and disadvantageously can provide current paths for leakage currents in bulk silicon and SOI CMOS devices having such dislocations.

SUMMARY OF INVENTION

[0003] The present invention provides structures and methods of manufacturing dislocation free stressed channels in bulk Si and SOI MOS (metal oxide semiconductor) devices by gate stress engineering with SiGe and/or Si:C. A MOS device comprises a substrate of either bulk Si or SOI, a gate dielectric layer over the substrate, and a stacked gate structure of SiGe and/or Si:C having stresses produced at the interfaces of SSi(strained Si)/SiGe or SSi/Si:C in the stacked gate structure. The stacked gate structure has a first stressed film layer of large grain size Si or SiGe over the gate dielectric layer, a second stressed film layer of strained Si or strained SiGe or strained Si:C over the first stressed film layer, and a semiconductor or conductor such as p(poly)–Si or silicide over the second stressed film layer.

[0004] The description herein discusses both stresses and strains, and it should be realized that stress and strain are related, with stress being proportional to strain, equaling a constant multiplied by the strain. Moreover, strong strain often creates dislocations in crystal structures. The description herein also refers to tensile stress which refers to stress applied in nFET channels and compressive stress

which refers to stress in a pFET channels.

[0005] The present invention: avoids dislocations generated in channels of bulk silicon and SOI (silicon on insulator) MOS (metal oxide semiconductor) devices; applies different types of stresses to nFET and pFET devices, separately; overcomes etch and clean processes of SiGe that can cause broken narrow electrical lines; applies stress by SiGe for ultra-thin SOI devices; overcomes dislocation generation increases at higher temperatures. This restricts the use of a thick metastable layer of strained Si (SSi) grown at relatively low temperatures (e.g. 550C) since SD RTA (source, drain, rapid thermal anneal); overcomes problems associated with the requirement that high Ge% SSi/SiGe require the SSi to be very thin in order to reduce the generation of dislocations. However, if the strained Si is too thin, (e.g. 5 nm, corresponding to 35% Ge critical thickness), the interface of SSi/SiGe can degrade mobility.

[0006] The present invention: provides structures and methods for making strained bulk Si and SOI CMOS devices by stressed gate engineering using stacked gates of SiGe and Si:C; allows the use of large Ge% and thickness of SiGe to produce large stresses due to the interfaces of SSi/SiGe or SSi/Si:C in the gates; provides stressed films of SSi/SiGe

and SSi/Si:C that are more stable due to the process of re-placement partial gate (refers to the replacement of a part of the poly in a gate, as disclosed and discussed herein below) occurring after high temperature processes (e.g. SD RTA); controls the stress in the channels of the devices by tuning Ge% or C% in SiGe or Si:C or by changing the thickness of the films; can be applied directly to bulk Si and SOI technologies without changing the conventional diffusion processes of the front-end-of-line (FEOL) pro-cesses.

BRIEF DESCRIPTION OF DRAWINGS

[0007] The foregoing objects and advantages of the present in-vention for structures and methods for manufacturing of dislocation free stressed channels in bulk silicon and SOI CMOS devices by gate stress engineering with SiGe and/or Si:C may be more readily understood by one skilled in the art with reference being made to the following detailed description of several embodiments thereof, taken in con-junction with the accompanying drawings wherein like el-ements are designated by identical reference numerals throughout the several views, and in which:

[0008] Figures 1 through 8 illustrate the fabrication process steps of a first embodiment of the present invention.

[0009] Figure 1 illustrates the structure after the completion of steps 1 and 2 that use conventional processes to form a gate oxide on a Si substrate and depositing a-Si or poly-Si, and annealing to obtain poly-Si with a large grain size.

[0010] Figure 2 illustrates the structure after step 3 involving oxidation and etching of the oxide on the large grain poly-Si layer until reaching ~10nm thickness.

[0011] Figure 3 illustrates the structure after step 4 involving depositing p(poly)-SiGe to form a stacked-gate layer.

[0012] Figure 4 illustrates the structure after step 5 that follows conventional processes for replacement gate to make devices with p-SiGe in the gates and spacers around the gates.

[0013] Figure 5 illustrates the structure after step 6 that involves depositing oxide, followed by CMP (chemical mechanical polishing), stopping on the top of the gates, and depositing a thin nitride layer.

[0014] Figure 6 illustrates the structure after step 7 that involves covering and patterning the pFETs with photoresist, etching the nitride and selectively etching the p-SiGe gates for the nFETs.

[0015] Figure 7 illustrates the structure after step 8 that involves removing the photoresist, selective epi of strained c-SiGe,

refilling the poly–Si in the nFETs and CMP stopping on the oxide.

[0016] Figure 8 illustrates the structure after step 9 that involves depositing a thin nitride layer and photoresist and generally repeating steps 6 and 7, but this time covering the nFETs and processing the pFETs.

[0017] Figure 9 illustrates a completed bulk silicon or SOI CMOS device with gate stress engineering with SiGe and/or Si:C.

[0018] Figure 10 illustrates a second embodiment of the present invention that follows process steps similar to the process steps of the first embodiment, but uses relaxed large-grain–size p–Si$_{1-x}$Ge$_x$ 100 instead of p–Si as the first gate layer or seed layer to grow the stressed film in the gate.

[0019] Figure 11 illustrates a third embodiment of the subject invention that can follow processes similar to the second embodiment, but wherein the seed layers for the nFETs and the pFETs have a different Ge fraction, e.g. for nFETs p–Si$_{1-x_n}$Ge$_{x_n}$ 110 and for pFETs p–Si$_{1-x_p}$Ge$_{x_p}$ 111.

[0020] Figure 12 illustrates a fourth embodiment of the present invention using a different process to make stressed layers in the gates by forming the gate stacked layer before gate patterning, to obtain the same structures as in the first, second and third embodiments.

[0021]   Figure 13 illustrates a fifth embodiment of the subject invention in a process using a bonded handle wafer with two single crystalline Si layers having a respective bonded oxide/Si interface and a thermal oxide/Si interface.

[0022]   Figure 14 illustrates a sixth embodiment of the subject invention with another process to make the structure with the double single crystal layers as shown in the fifth embodiment. This process uses regrowth of single crystal from an a-Si layer, starting the a seeds near the gates.

[0023]   Step 1 starts with a conventional wafer on a single crystal Si (c-Si) substrate 140, and follows conventional processes to make a gate oxide layer 142 on the Si substrate, and then deposits a thin layer (e.g. thickness ~25 nm) of a-Si 144, as shown in Figure 14.

[0024]   Figure 15 illustrates the structure after step 2 involving depositing and patterning the photoresist, etching the a-Si, and etching the gate oxide.

[0025]   Figure 16 illustrates the structure after step 3 involving removing the photoresist and depositing a-Si (~25nm).

[0026]   Figure 17 illustrates the structure after step 4 involving patterning the photoresist such that it still covers both the nFET regions and the pFET regions, and etching the a-Si down to the gate oxide in order to isolate the nFET re-

gions and the pFET regions for regrowth of crystal Si.

[0027] Figure 18 illustrates the structure after step 5 involving annealing to recrystalize the a–Si layer to form single crystal Si.

DETAILED DESCRIPTION

[0028] Figures 1 through 8 illustrate the fabrication process steps of a first embodiment of the present invention.

[0029] Figure 1 illustrates the structure after the completion of steps 1 and 2. Step 1 uses conventional processes to form a gate oxide 12 on a Si substrate 10 (alternate embodiments can employ an SOI technology) of a wafer, and step 2 involves depositing a–Si (amorphous silicon) or poly–Si, and annealing the a–Si or poly–Si to obtain poly–Si 14 with a large grain size. If the grain size is approximately 200 nm, as shown in Figure 1, for a 50 nm gate device (shown as Lpoly = 50 nm), there is a 75% probability of not seeing a grain boundary 16 in the lateral direction of the gate, as illustrated by Figure 1. The grain boundaries assist in relieving stress in the material.

[0030] Figure 2 illustrates the structure after step 3 involving oxidation and etching the oxide on the large grain poly–Si layer until reaching ~10nm thickness.

[0031] Figure 3 illustrates the structure after step 4 involving de-

positing p(poly)–SiGe to form a stacked–gate layer 40.

[0032] Figure 4 illustrates the structure after step 5 that follows conventional processes for replacement gate to make devices with p–SiGe 40 in the gates and spacers 42 around the gates. Note that all dopants are in place and annealed to become active and no further diffusion is needed for dopant activation.

[0033] Figure 5 illustrates the structure after step 6 that involves depositing oxide 50, followed by CMP (chemical mechanical polishing), stopping on the top of the gates, and depositing a thin nitride layer 52 to prevent epi (epitaxial crystal growth), on the top of the gates when the nFETs and pFETs are processed separately.

[0034] Figure 6 illustrates the structure after step 7 that involves covering and patterning the pFETs 60 with photoresist 64, etching the nitride 52 and selectively etching the p–SiGe 40 gates at 66 for nFETs 62. The purpose of covering the pFETs is to produce different levels or types of stresses in the nFET devices and the pFET devices, separately.

[0035] Figure 7 illustrates the structure after step 8 that involves removing the photoresist 64, selective epi (epitaxial crystal growth) of strained c–SiGe (single crystal) 70 (<critical thickness and may need in–situ doping for the gate), re-

filling the poly–Si at 72 in the nFETs 62 and CMP stopping on the oxide 50, and perhaps etch back a little in the nFETs 62.

[0036] Figure 8 illustrates the structure after step 9 that involves depositing a thin nitride layer 80 and photoresist 82 and generally repeating steps 6 and 7, but this time covering the nFETs 62 and processing the pFETs 64; using strained Si:C 84 to replace SiGe for the pFETs and then refilling poly–Si at 86 and CMP stopping at the oxide 50. Figure 8 illustrates the grain boundary 16 continuing into the strained Si:C. Figure 8 illustrates the completed stacked gate structure of the first embodiment, and after this step, conventional processes are used to form silicide for the gates and finish the back–end–of–line (BEOL) work.

[0037] Another option involves covering the nFET regions and doing carbon implantation into the pFET gates, and annealing at 700C–850C to produce tensile stress in the implanted areas in the pFET gates.

[0038] Figure 9 illustrates a completed strained bulk silicon or SOI MOS device with gate stress engineering using a stacked gate of SiGe and/or Si:C to produce stresses produced by the interfaces of SSi/SiGe or SSi/Si:C in the stacked gate structure. Figure 9 illustrates that the de-

vices can be fabricated on a substrate of either bulk semi-conductor (Si) 10 or semiconductor on insulator (SOI) 90, and include a gate dielectric layer on top of the substrate, and a stacked gate structure having a first semiconductor or conductor stressed film layer 14 of single crystal or large grain size Si or SiGe over the gate dielectric layer 12, a second semiconductor or conductor stressed film layer 70 or 84 of strained c-SiGe or strained c-Si:C over the first stressed film layer, and a semiconductor or conductor film 72 or 86 such as p-Si over the second stressed film layer, and dielectric spacers 42 around the stacked gate structure. The stress/strain in the gates can be produced in different embodiments by different materials or by different percentages of materials.

[0039] Figure 10 illustrates a second embodiment of the present invention that follows process steps similar to the process steps of the first embodiment, but uses relaxed large-grain-size p-Si$_{1-x}$Ge$_x$ 100 instead of p-Si as the first gate layer, which is used as a seed layer to grow the stressed film in the gate. This layer is strained after the selective epitaxial growth step. The percentages of materials can be changed in different embodiments to obtain different stresses. In step 4 of the first embodiment, p-SiGe depo-

sition is replaced by p–Si deposition. Similarly, in steps 7 and 8 of the first embodiment, the selective etching steps of p–SiGe become selective etching of p–Si. In this case, in the gate of nFETs 102, $Si_{1-y}Ge_y (y>x)$ 106 is grown, and in the gate of pFETs 104, $Si_{1-z}Ge_z (z<x)$ 108 is grown. Therefore, the process results in compressive stress in pFET channels and tensile stress in nFET channels. For the pFETs, the process can also use Si:C instead of $Si_{1-z}Ge_z (z<x)$, although SiGe has a better thermal stability than Si:C. The value of x can also be used to adjust the pFET Vt (threshold voltage). Usually, this requires less halo doping in the pFET channel which can further improve pFET performance. Figure 10 illustrates the final resultant structure after all of the process steps are performed. The $Si_{1-x}Ge_{x_p}$ 100 is the seed layer for the parts of the gates above it, and this layer is strained after the selective epitaxial growth.

[0040] Figure 11 illustrates a third embodiment of the subject invention that can follow processes similar to the second embodiment, but wherein the seed layers for the nFETs 112 and the pFETs 114 have a different Ge fraction, e.g. for nFETs 112 $p–Si_{1-x}nGe_{xn}$ 110 and for pFETs 114 $p–Si_{1-x}pGe_{x_p}$ 111. This process can use conventional pro–

cesses that cover the pFET and the nFET regions, separately. In this case, in the gates of the nFETs, $Si_{1-y}Ge_y$ (y>xn) 116 is grown and in the gates of pFETs, $Si_{1-z}Ge_z$ (z<xp) 118 is grown. Therefore, the process obtains compressive pFET channels and tensile nFET channels. For the pFETs, the process can also can use Si:C instead of $Si_{1-z}Ge_z$ (z<x) 118, although SiGe has a better thermal stability than Si:C. The value of x also can be used to adjust the pFET Vt. Usually, this requires less halo doping in the pFET channels which can further improve pFET performance. Figure 10 illustrates the final resultant structure. The $Si_{1-xn}Ge_{xn}$ 110 seed layer for the part of gate above this seed layer and this seed layer are strained after the selective epitaxial growth. The $Si_{1-xp}Ge_{xp}$ 111 seed layer for the part of gate above this seed layer and this seed layer are strained after the selective epitaxial growth.

[0041] Figure 12 illustrates a fourth embodiment of the present invention using a different process, probably easier, to make stressed layers in the gates by forming the gate stacked layer 120 before gate patterning, as shown in Figure 12, to obtain the same structures as in the first, second and third embodiments. Simulations have shown that although structure-wise they are the same, the stresses

produced by the first, second and third embodiment processes are ~30% larger than those generated by the fourth embodiment. The strained SiGe or strained Si:C layer could have different stress levels, different stress types, and different Ge fractions in the nFET and pFET regions, separately. The large–grain–size p-Si 14 or p-SiGe 100 as seed for the epi SiGe or Si:C layer could have different stress levels, different stress types, and different Ge fractions in the nFET and pFET regions, separately.

[0042] Figure 13 illustrates a fifth embodiment of the subject invention. One drawback for the first through fourth embodiments is the difference of crystalline orientations among grains in the stacked–gates. This may cause performance variations of narrow width devices since there may be only one grain in their gate. To avoid this problem, a process can use a bonded handle wafer 130 with two single crystalline Si layers 132, 134 having a respective bonded oxide/Si interface 133 and a thermal oxide/Si interface 135 as shown in Figure 12. This structure can be used to replace the structure shown in step 2 of the first embodiment, and then follow the rest of the steps of the first through fourth embodiments to make strained silicon devices. To take advantage of Smart–Cut (which is a

method to cut the wafer after bonding by employing an H implant to damage the single crystal Si 132 and then cutting/breaking along the damaged implant), the process can deposit a thin metal or silicide layer on the gate oxide 131 before bonding to the handle wafer 130. The thin metal or silicide layer can be used to tune the threshold voltage Vt of the devices, or to obtain a thinner electrical dielectric thickness for a given thickness of gate oxide.

[0043] Figure 14 illustrates a sixth embodiment of the subject invention with another process to make the structure with the double single crystal layers as shown in the fifth embodiment. This process uses regrowth of single crystal from an a-Si layer, starting the a seeds near the gates.

[0044] Step 1 starts with a conventional wafer on a single crystal c-Si substrate 140, and follows conventional processes to make a gate oxide layer 142 on the Si substrate, and then deposits a thin layer (e.g. thickness ~25 nm) of a-Si 144, as shown in Figure 14.

[0045] Figure 15 illustrates the structure after step 2 involving depositing and patterning the photoresist 150, etching the a-Si at 152, and etching the gate oxide at 154.

[0046] Figure 16 illustrates the structure after step 3 involving removing the photoresist 150 and depositing a-Si

(~25nm) 160, and also shows the seed 162 for regrowth of single crystal.

[0047] Figure 17 illustrates the structure after step 4 involving patterning the photoresist such that it still covers both the nFET regions 172 and the pFET regions 174, and etching the a-Si at 170 down to the gate oxide in order to isolate the nFET regions 172 and the pFET regions 174 for re-growth of crystal Si at 162, which is also the region of STI (shallow trench isolation), such that removal of the gate oxide is not a problem.

[0048] Figure 18 illustrates the structure after step 5 involving annealing at 570C for 10 hours to recrystalize the a-Si layer to form single crystal Si 180 (Brian J. Greene et al). In this condition, a-Si can regrow as long as ~1um in the lat-eral direction, and usually the total width of the device is less than 0.5 um for high performance devices. After this step, the processes described in the first through fourth embodiments can be used to make devices with the same crystalline orientations in their gates. The position of the seed for regrowth of single crystal is also the place of STI such that removal of the gate oxide is fine.

[0049] While several embodiments and variation of the present invention for structures and methods for manufacturing of

dislocation free stressed channels in bulk and SOI MOS devices by gate stress engineering with SiGe and/or Si:C are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.